IN THE CLAIMS:

Please amend the claims as follows:

Claim 1. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type within said substrate for forming a drain of a first MOS transistor;

a second region of the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

Claim 2. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type within said substrate for forming a drain of a first MOS transistor;

a second region of the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on of said first MOS transistor, and

wherein the channel length of said first MOS transistor is longer than the channel length of said second MOS transistor to increase the drain base voltage of said first MOS transistor.

Claim 3. (**Previously Presented**) The semiconductor structure of claim 1, further comprising:

a pre buffer circuit coupled to a gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

Claim 4. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type with said substrate for forming a drain of a first MOS transistor;

a second region of he the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on of said first MOS transistor;

a first channel region disposed between said first and second regions of said first MOS transistor; and

a second channel region disposed adjacent to said third region of said second MOS transistor,

wherein said first channel length of said first channel region is longer than the channel length of said second channel region to increase the drain base breakdown voltage of said first MOS transistor.

Claim 5. (**Canceled**)

Claim 6. (**Canceled**)

Claim 7. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a pair of first regions of a second conductivity type within said substrate for defining a first channel region of the second conductivity type for a first MOS transistor;

a pair of second regions of the second conductivity type within said substrate for defining a second channel region of the second conductivity type for a second MOS transistor, wherein the

channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn on speed of said first MOS transistor; and

a third region of the first conductivity type between the source side of said first regions and the source side of said second regions for surrounding said first MOS transistor with an additional pick up diffusion to further restrain the turn on speed of said first MOS transistor.

Claim 8. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source of a second MOS transistor, wherein

a P+ region is disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

Claim 9. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a p type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source of a second MOS transistor,

wherein a P+ region is disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on speed of said first MOS transistor, and

wherein the channel length of said first MOS transistor is longer than the channel length of said second MOS transistor to increase a drain base breakdown voltage of said first MOS transistor.

Claim 10. (**Previously Presented**) The semiconductor structure of claim 8, further comprising:

a pre buffer circuit coupled to a gate of the first MOS transistor; and

an output pad coupled to said first region of the first MOS transistor.

Claim 11. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a p type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source of a second MOS transistor,

wherein a P+ region is disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on speed of said first MOS transistor;

a first n channel region having a first channel length and disposed between said first and second regions of said first MOS transistor; and

a second n channel region having a second channel length disposed adjacent to said third region of said second MOS transistor,

wherein said first channel length is longer than said second channel length to further increase the drain base breakdown voltage of said first MOS transistor.

Claim 12. (**Canceled**)

Claim 13. (**Canceled**)

Claim 14. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit comprising:

a p type substrate forming a base for said semiconductor structure;

a pair of first N+ regions within said substrate for defining a first n channel region for a first MOS transistor;

a pair of second N+ regions within said substrate for defining a second n channel region for a second MOS transistor, wherein the channel length of said first channel is greater than the channel length of said second channel; and

a third P+ region between the source region of said first N+ regions and the source region of said second N+ regions for surrounding said first MOS transistor with an additional pick up diffusion to further restrain the turn on of said first MOS transistor.

Claim 15. (**Canceled**)

Claim 16. (**Currently Amended**) ~~The semiconductor structure of claim 15~~ A semiconductor structure for electrostatic discharge (ESD) protection of a metal oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad and an internal circuit of said integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel formed between a pair of first regions of a second conductivity type within said substrate for a first MOS transistor; and

a second channel formed between formed between a pair of second regions of a second conductivity type within said substrate for a second MOS transistor,

wherein an additional pick up diffusion region is disposed between the source region of said first regions and the source region of said second regions for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on of said first MOS transistor,

wherein the channel length of said first channel is longer than the channel length of said second channel to increase a drain base breakdown voltage of said first MOS transistor.

Claim 17. (**Previously Presented**) A semiconductor structure for electrostatic discharge (ESD) protection of a high voltage tolerant I/O cells with stacked NMOS or PMOS integrated circuit, said semiconductor structure connected between a pre driver circuit and an input/output pad of said integrated circuit and comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel formed between a pair of first regions of a second conductivity type within said substrate for a first MOS transistor which is stacked on a third MOSFET of a second conductivity type; and

a second channel formed between a pair of second regions of a second conductivity type within said substrate for a second MOS transistor which is stacked on a fourth MOSFET of a second conductivity type, wherein

an additional pick up diffusion region is disposed between the source region of said first regions and the source of said second regions for surrounding said first MOS transistor with an additional pick up diffusion to restrain the turn on of said first MOS transistor.

Claim 18. (**Previously Presented**) The semiconductor structure of claim 17, wherein the channel length of said first channel is longer than the channel length of said second channel to increase the drain base breakdown voltage of said first MOS transistor.

Claim 19. (**Canceled**)